MTC-30521

VAN Interface

Data Sheet

Application Specific Standard Products

Features

- **Line Interface Circuit for Automotive Multiplex Systems**
- **Fully Integrated Support for the VAN Protocol (layer 1 of the OSI model)**
- **Integrates:**
  - **Interface protection**
  - **Line biasing**
  - **Transmitter**
  - **Receiver**
  - **Power Supply Regulator for Local Node**
  - **Wake-Up / Sleep System**
- **Hardware Support for Bus Collision Detection**
- **Data Rates from 10k to 160kbits/second**
- **Multi-Master / Multi-Slave Configurations, as well as Master-Slave**
- **Integrated Protection against Automotive Interference Pulses, including Load-dump**
- **High-voltage BICMOS Technology**

Product Description

The chip is designed to be used in a car multiplexing system in bus collision mode, using the VAN protocol according to ISO standard 11519-3, at a maximum transmission speed of 160 kHz.

The circuit consists of the following blocks:
- differential line transmitter
- differential line receiver with built-in filtering and digital interface
- sleep and wake up system
- 5.6 V power supply

Normal Operation Mode

The network consists of several nodes connected to a two-wire bus. The chip acts as the interface between the bus wires and the digital parts controlling communication. The bus sees all nodes as physically identical. The difference between nodes is in the controlling part which defines whether a node is a master or a slave. There can be only one master on a network.For this interface chip the difference between master and slave only becomes important during sleep and wake up mode. This will be described further on.

The interface chip is directly connected to the bus wires on the two pins called Data and DataB. These two pins are the outputs of the line transmitter, and are also the inputs of the line receiver. Eventually an impedance balance can be added externally at these two pins.

ALCATEL

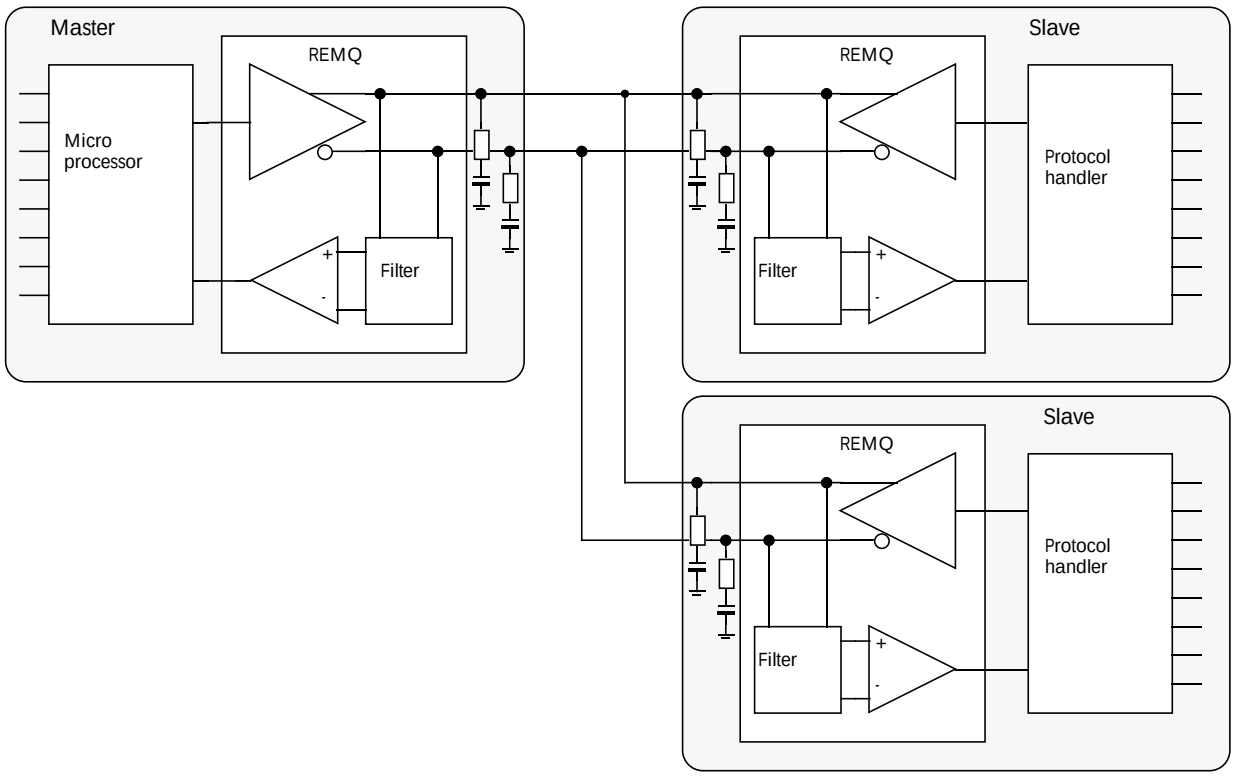


Fig.1: Basic Configurations of the Network

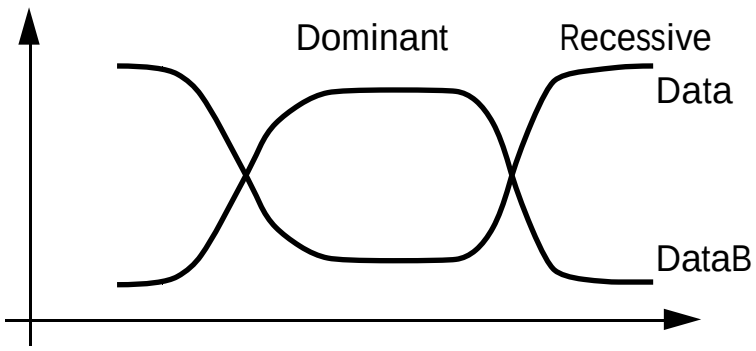


Fig.2: Typical Bus Signals

• **Transmitter**

The line transmitter consists of two push-pull current source outputs : one is controlled by the input DE, the second is controlled with the inverse signal. The output transitions have to have a well defined and smooth slope when loaded with a wide range of networks, composed of R's, L's and C's. Furthermore, the slopes of the two outputs have to match each other.

In this way the two bus wires are driven with complementary signals, thus minimizing the common mode radiation. This is shown in figure 2.

Each output has a 50mA current source, defining the dominant state and a 1 mA current source defining the recessive state. The 50 mA current source can be switched on and off to transmit data to the bus wires. When a node is listening, the line transmitter is kept in its recessive state. When a node is transmitting data to the bus, the line transmitter switches between dominant and recessive state, thus overdriving all nodes which are in the recessive state. While the chip is in sleep mode, all current sources are disabled and remain high impedant. This functionality is summarized in table 1 and figure 3. The input signal SleepB puts the circuit in sleep mode when connected to ground.

Table 1: Functional State Diagram

SleepB	DE	DH1	DL1	DH2	DL2
1	0	1	50	50	1
1	1	1	HI	HI	1
0	X	HI	HI	HI	HI

HI = high impedant

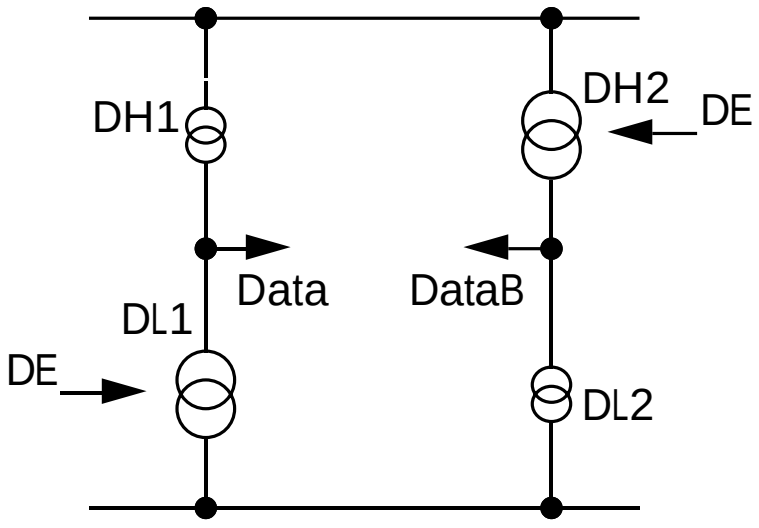


Fig.3: Transmitter Current Sources

• **Receiver**

The line receiver is always active during normal operation, independent of the state of the transmitter. Basically the receiver part consists of an on-chip passive (first order) low pass filter, followed by three comparators in parallel. The outputs of these comparators pass to a small block of logic and are then transferred to the controller chip. The implemented filter is fully symmetrical, thus generating the internal signals Ri and Rib from the signals Data and DataB. Ri and RiB are fed to the inputs of the comparators. From these three comparators, one has its two inputs connected to Ri and RiB. The two other comparators have only one input connected to either Ri or RiB, while the other input is connected to an on chip reference voltage, indicated as Vpol. The value of this voltage is about half the output voltage of the transmitter. This ensures that, when the transmission is disturbed on one of the wires, the communication can still go on via the transmission on the other wire and one of the two supplementary comparators.

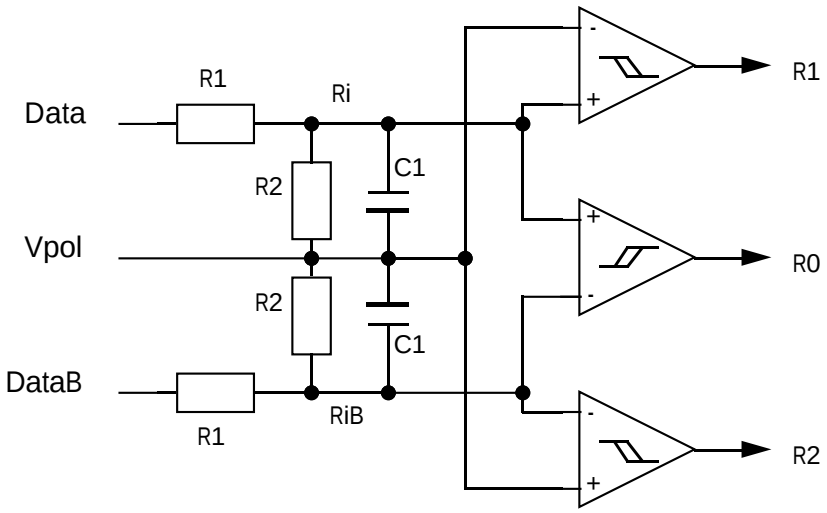


Fig. 4: Receiver Section

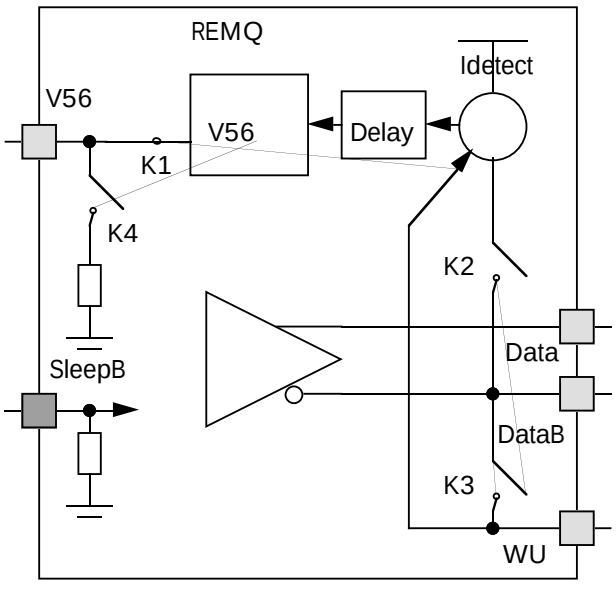


Fig. 5: Sleep Circuit during Normal Operations

Sleep Mode Operation

An important function of the multiplexing system is its ability to go into a sleep mode. At this moment the power consumption is reduced to the minimum. The system can wake up again in two different ways.

Although all interface chips are physically identical, the functionality of the chip is different for a master and a slave node. Figure 5 shows the most important circuits with regard to the sleep mode. On node DataB there are two switches, one to Vbat via a current sensor and one to the pin WU. Furthermore, the input SleepB is used to put the circuit in sleep mode, at which time the V56 regulator will be shut down.

Following is a detailed description of the behavior of a master and a slave node. Figure 5 illustrates the state of all switches during normal operation; this is identical for a master and a slave node. Figure 6 shows a system during sleep mode. Figure 7 and 8 illustrate the possible sequences to go from sleep mode to normal mode and back.

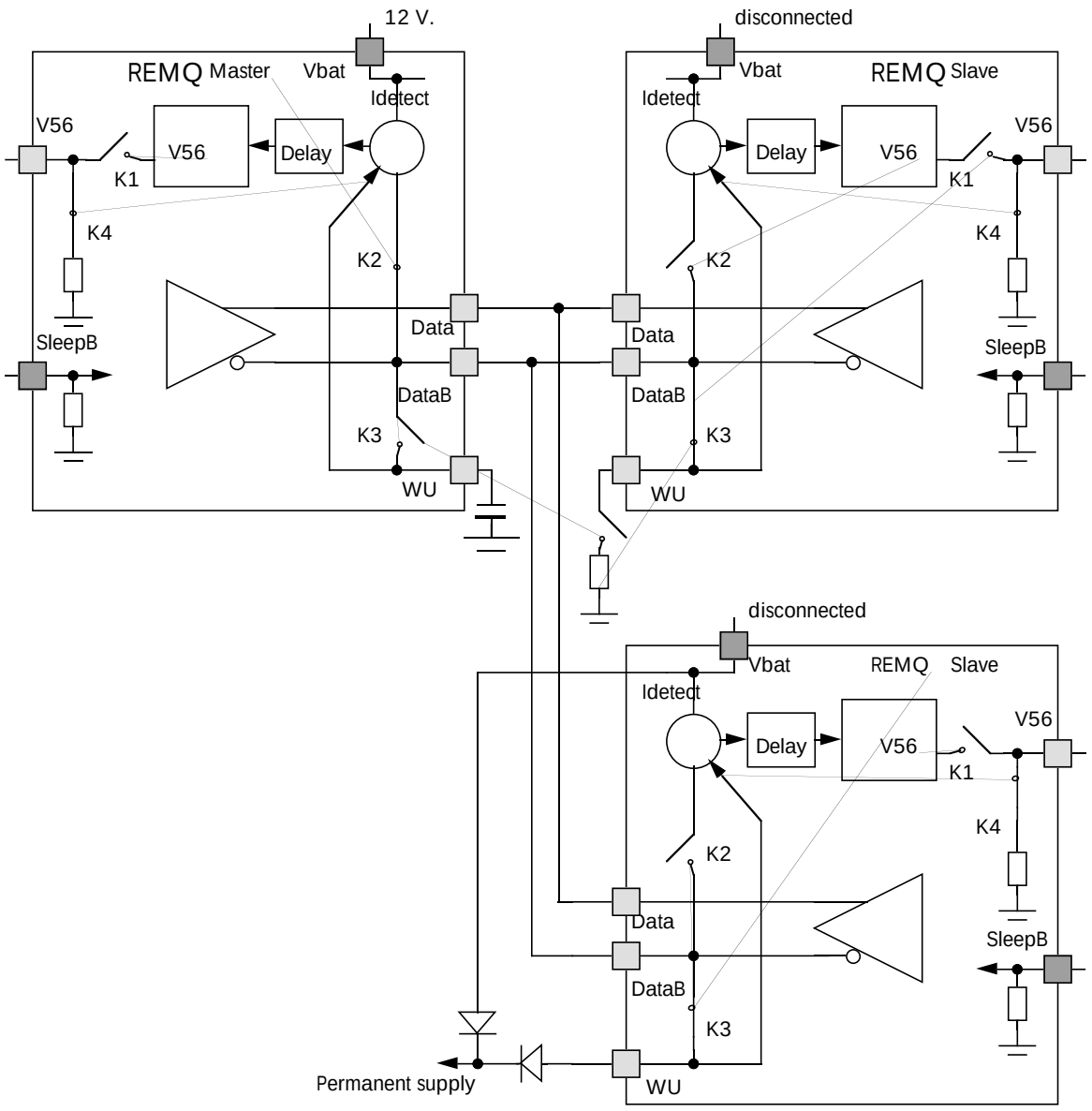


Fig. 6: System Configuration in Sleep Mode

- **Entering Sleep Mode**

The interface chip in the master node is permanently connected to the supply Vbat. The system is put in sleep mode by pulling the pin SleepB of the master node to ground. This condition will disable the voltage regulator V56 (K1 opens, K4 closes) in the master. At the same time the switch K2 closes which connects Vbat with the DataB wire. The transmitter is disabled and rendered highly impedant.

When the V56 regulator of the master is disabled, the Vbat of all slaves is disconnected from the supply by an external circuit (e.g. by a relay which is controlled by V56 of the master). This also cuts off the V56 of the slaves. From this moment on the slaves are only supplied via the pin DataB. This is the difference between a master and a slave.

Because the Vbat of the slaves is disconnected, the switch K3 closes, connecting DataB with the pin K3. The system is now in sleep mode.

- **Wake up through Current Detection**

When, at a particular slave node, the pin WU is connected to ground (eventually via a resistor) a current will flow from Vbat at the master node, through the DataB wire, to ground. When this current is above a well defined value, this will be detected in the master node. When this current is flowing for a period tds the V56 regulator in the master is activated. The period tds is defined by the interface chip and an external capacitor connected to pin WU at the master node. When V56 is active again, the microprocessor in the master node will pull high the pin SleepB. This will open the switch K2. The master is now in normal operation again.

Since the V56 in the master is activated again, the pin Vbat in the slaves is reconnected to the supply. In all slaves the pin SleepB is connected to Vbat. Therefore, from the moment the Vbat is connected, the slave is in normal operation again. Switch K3 is therefore opened.

Table 2 illustrates the different states for both a master and a slave.

Table 2: State Diagram for Sleep - Wake-up System

MASTER NODE	Sleep mode	Normal operation
K1	open	closed
K2	closed	open
K3	open	open
K4	closed	open
WU	loaded with cap.	loaded with cap.
SleepB	"0"	"1"
Vbat	connected	connected
SLAVE NODE	**Sleep mode**	**Normal operation**
K1	open	closed
K2	open	open
K3	closed	open
K4	closed	open
WU	contact to ground	contact to ground
SleepB	"0"	"1"
Vbat	disconnected	connected

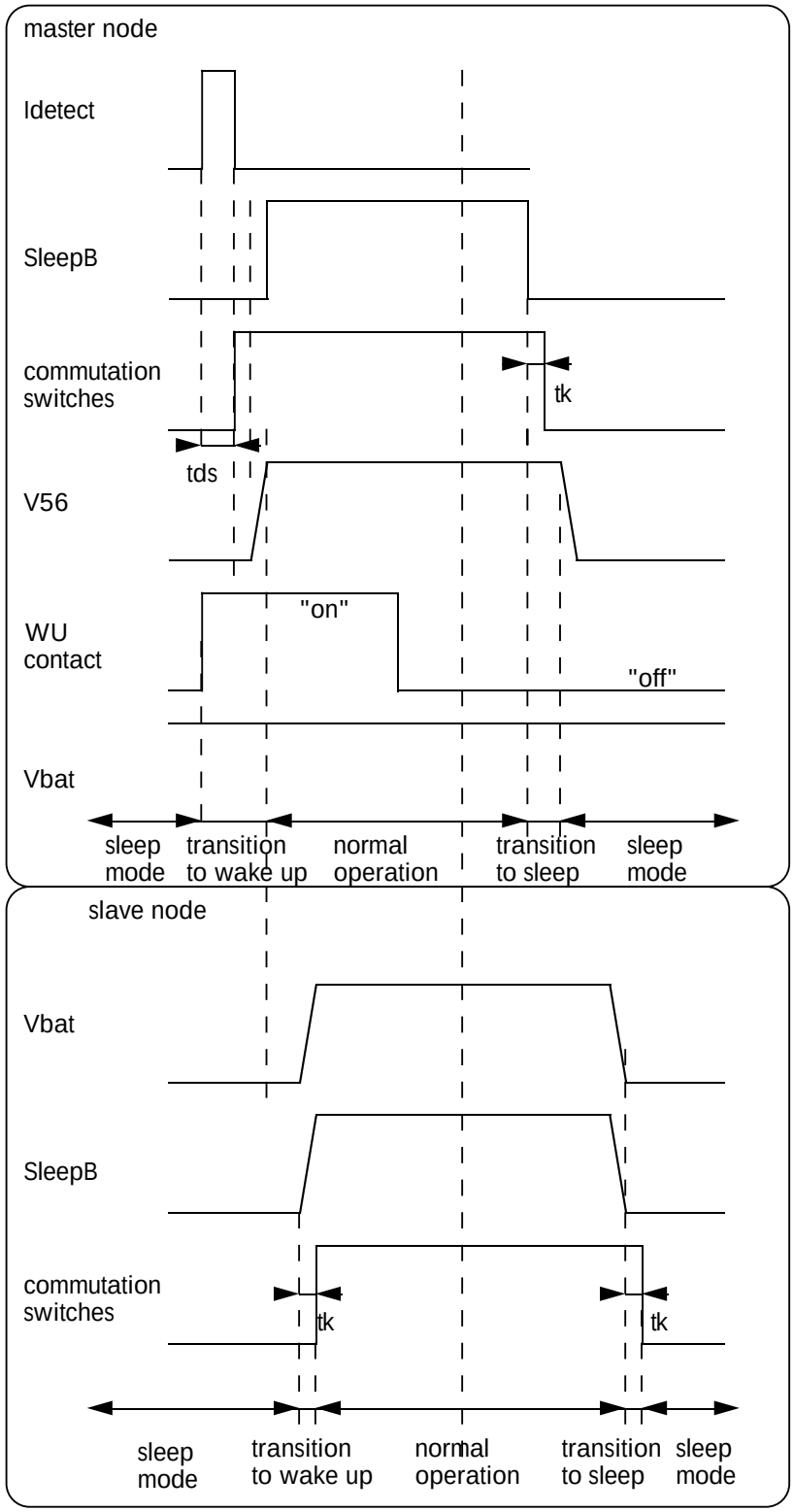


Fig. 7: Wake-up through Current Detection

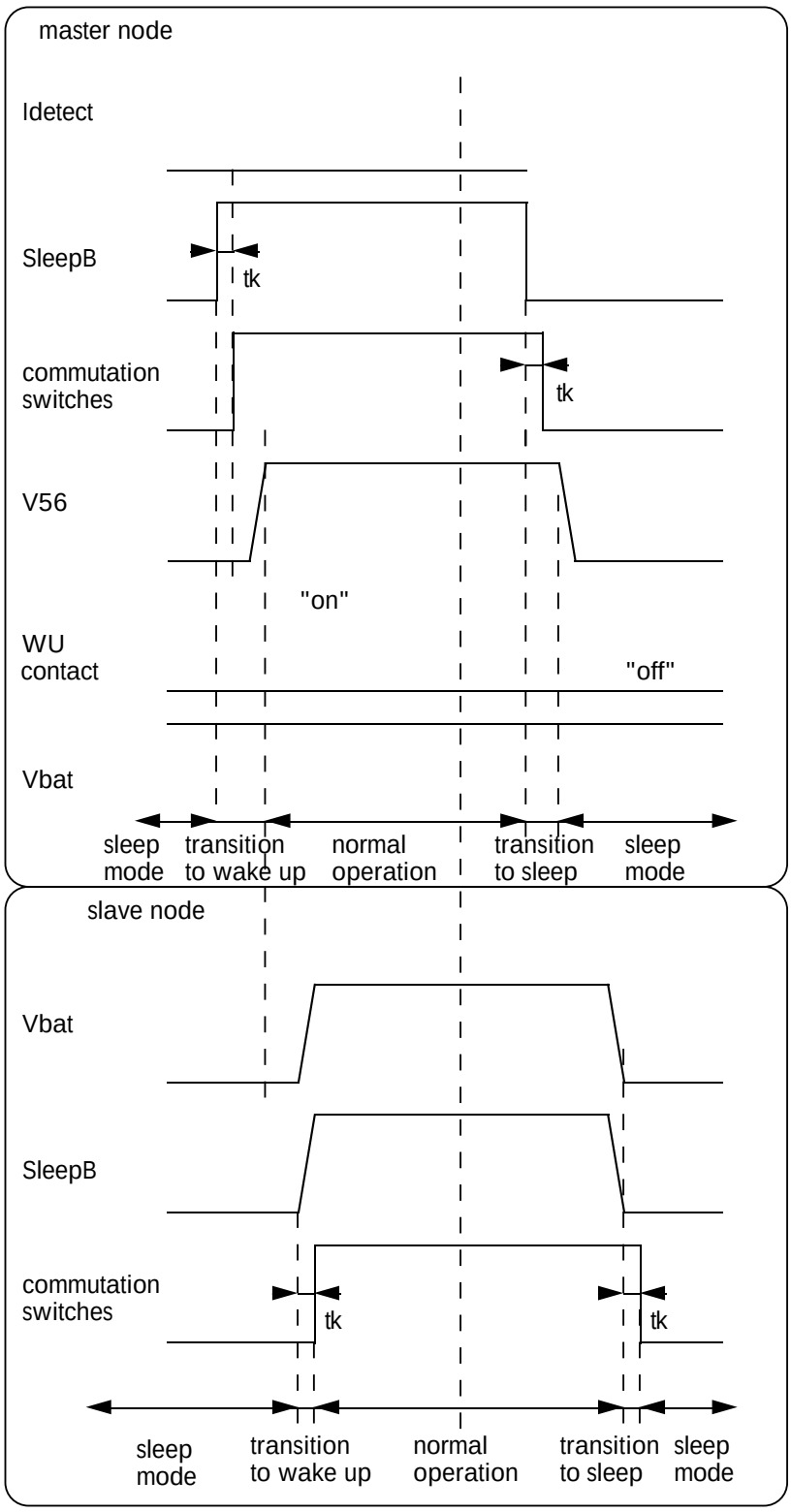


Fig. 8: Wake-up through SleepB Activation

- **Wake-up through SleepB Activation**

The system can also be activated by pulling high the pin SleepB of the master. At that moment the V56 regulator will be enabled and the master is in normal operation again. Powering up the V56 regulator will also connect the Vbat of the slaves again, putting the slaves back in normal mode.

- **Permanent Supply at a Slave Node**

Circuits located at a slave node and which need a permanent supply, even during sleep mode, can be connected as shown in figure 6. The current consumption of this circuit has to be low enough to avoid the master detecting this as a current to restart the system.

Voltage Regulator

A voltage regulator which generates 5.6 Volt is implemented on the chip. This regulator is supplied via the pin Vbat. During sleep mode the regulator will be disabled via the pin SleepB. At that moment the pin V56 is connected to ground via a resistor.

The circuit is a low drop voltage regulator, which implies that, for stability reasons, the output has to be loaded with a minimum capacitance.

Environmental Conditions

The chip is intended to be used in an automotive environment. This implies several specific requirements for the circuit. All requirements are valid for the full temperature range and for every possible state of the circuit. Following is a list of extreme environmental conditions:

The pins Data, DataB and Vbat can be directly connected to a permanent voltage of +24 Volt, to the ground, and have to withstand the voltages described in table 3 without destruction of the device. Parametrical characteristics will not be guaranteed under these conditions.

To avoid extreme power dissipation on the chip, the dominant output current sources will be disabled when extreme voltages are applied to the pins Data and DataB. The voltage level at which the disabling becomes active are above +10 V and below - 5 V This is to ensure that the line transceiver will not be disabled in the range from - 5 to +10 V. The disabling for the two outputs is independent of each other: a disabling of one output will not influence the performance of the other one.

The voltage regulator V56 is current limited. A short circuit to ground will not destroy the device by overcurrent. However it is clear that the power dissipation can become excessive.

The outputs of the line transmitter have to be independent. When one is short circuited to ground, to the supply voltage, or is open, this should not influence the performance of the other output.

Table 3: Environmental Conditions

Amplitude	Duration	Rg	Period	Number of pulses
50 V - 50 V	400 ms 100 ms	2 10	1mn 1mn	5 50

Pinout and Packaging

1. Pinout

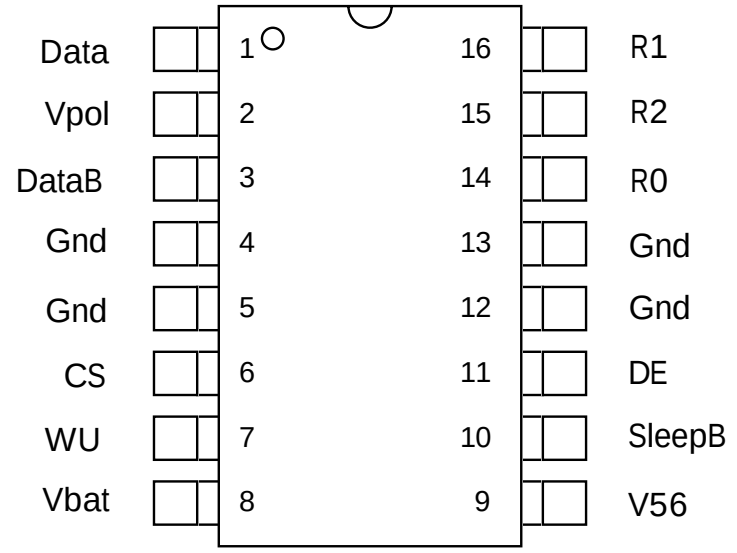


Fig. 9: Pin Configuration

2. Pin Description

Nr.	Name	Type	Description
1	Data	interface	positive interface pin
2	Vpol	analog out	reference voltage
3	DataB	interface	negative interface pin
4	Gnd	supply	ground reference pin
5	Gnd	supply	ground reference pin
6	CS	analog in	current setting input
7	WU	analog I/O	wake up pin
8	Vbat	supply	supply voltage
9	V56	analog out	supply output voltage
10	SleepB	digital in	sleep input
11	DE	digital in	transmit data in
12	Gnd	supply	ground reference pin
13	Gnd	supply	ground reference pin
14	R0	digital out	receive data R0
15	R2	digital out	receive data R2
16	R1	digital out	receive data R1

3. Packaging

Package Name	Package Code	Alcatel Microelectronics Drawing no	JEDEC Outline DWG
16 pins PSOP 300 mils	SO16 B	87-0034	MS-013

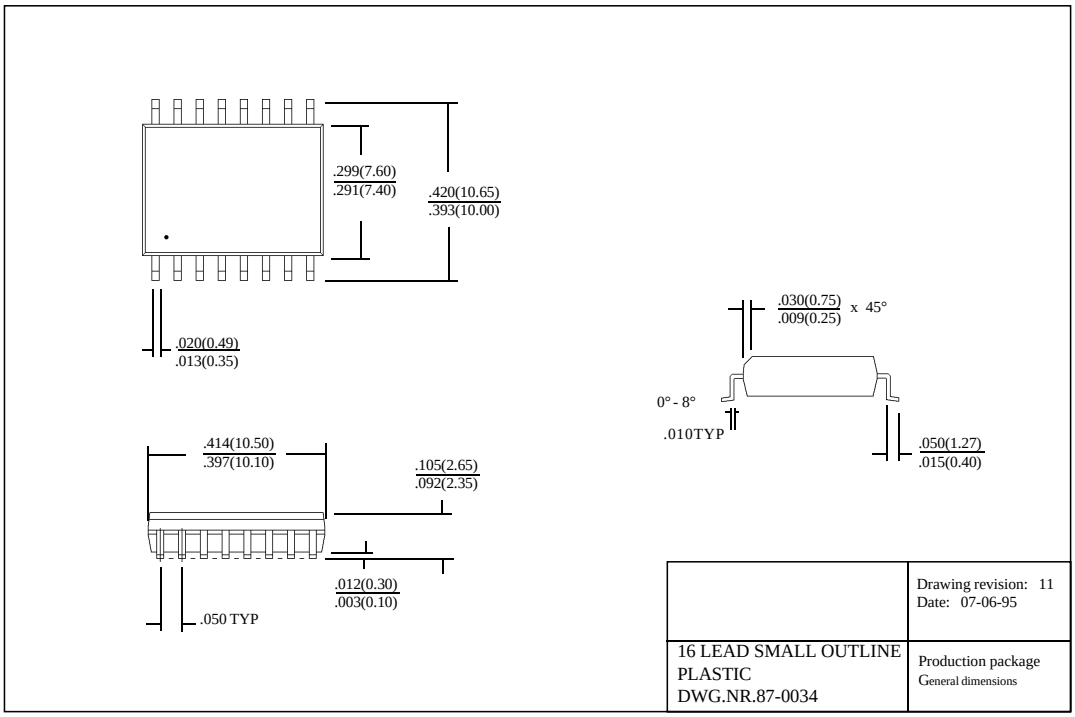


Fig. 10: Package

4. Marking

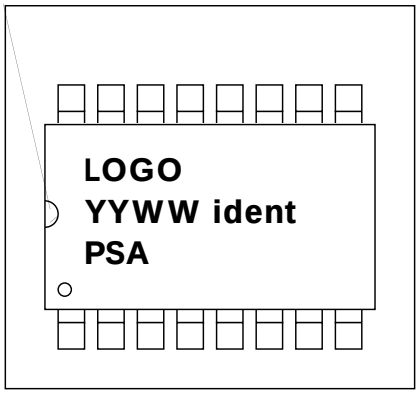


Fig. 11: Topside Marking

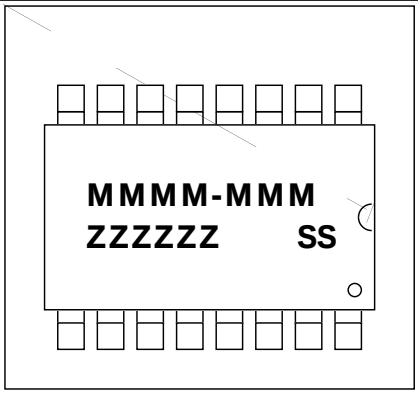


Fig. 12: Backside Marking

LOGO : Micro-signature Alcatel.
YYWW : assembly year and week.
ident : REMQ
SS : Assembly source code.
MMMM-MMM : Alcatel Microelectronics product name.
ZZZZZZZ : wafer lot identification.

5. Delivery

5.1 Delivered in tubes

44 devices per tube

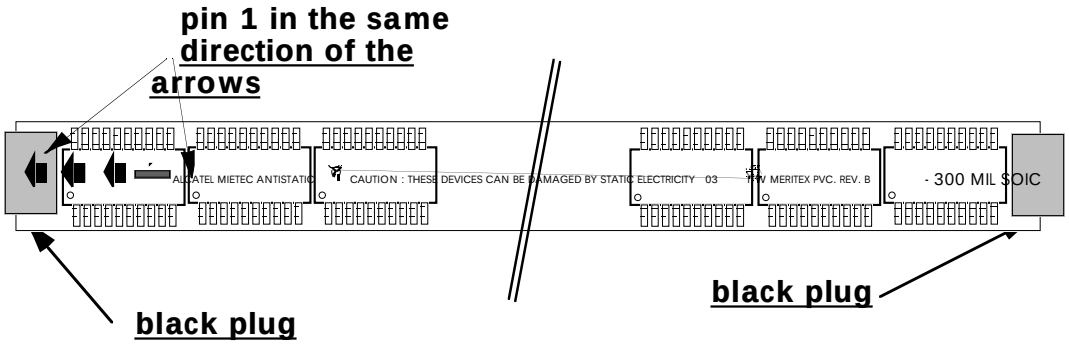


Fig. 13: SOIC Tube

5.2 Delivered tape on reel

The plastic small outline (SO), can be placed in tape on reel, eventually in combination with dry pack.

All used materials and procedures are in line with the related EIA, IEC documents.

IEC 286-3 - packing of components for automatic handling

EIA-481-2 - 16 and 24 mm embossed carrier taping of surface mount components for automatic handling

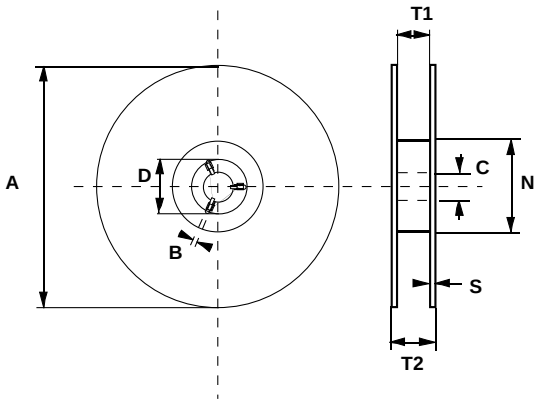


Fig. 14

Reels (Fig. 14)

Tape width	A	N	T1	T2	D	B	C	S
	+0.5 -0.5	+0.5 -0.5	+0.4 -1.6	+0.4 -0.6	+0.2 -0.2	+0.0 -0.5	+0.2 -0.2	typ
16	330	62	18	22	30.0	2	13	2.0

(All figures in mm)

Carrier tapes

Carrier tapes with width of 12, 16, 24, 32 or 44mm are used.

Material : Conductive polystyrene - black
Thickness : 200 - 400um
Tensile strenght : 19 - 25 Mpa
Elongation at break : 40 - 45%
Surface resistance : 10E4 - 10E6 ohms/sq
Vicat softening point : 90 - 98°C

Dimensions for 12, 16 or 24mm tape (All dimensions in mm) (Fig 15).

W : 12 +/- 0.3 or 16 +/- 0.3 or 24 +/- 0.3
D1min : 1.5
E1 : 1.75 +/-0.10
P0 : 4.0 +/-0.10
S1min : 0.6

Cover tape

Cover tapes with width of 9.3, 13.5, 21.5, 25.5, 37.5mm are used in relation to the tape width.
Material :
static dissipative polyester temperature sensitive tape
First layer : Transparent polyester
Second layer : Polyethylene
Total thickness : 0.060 mm
Tensile strength : 110 N/cm
Surface resistivity : 1.2x10E12 ohm/SQ
Elongation at break : 91%

The clearance between the ends of the terminals or body of the component to the sides and depth of the cavity (A0, B0, C0) must be within 0.05mm min and 0.50mm max for 12mm tape, or within 0.15mm min and 0.9mm max for 16mm tape, or within 0.15mm min and 1.0mm max for 24, 32 or 44mm tape.

The cavities of the 44, 68 and 84 pins PLCC (PC) and PQFP (PQ) devices will have a platform supporting the body of the package making sure the lead tip is not touching the cavity.

General

All components are located in the cavity with pin 1 adjacent to the round sprocket holes.

The components are packed with the terminations facing the bottom of the embossed carrier.
There is a leader (start) of 230mm minimum which may consist of carrier and/or cover tape followed by a minimum of 160mm of empty carrier tape sealed with cover tape.

There is a tailer (End) of 160mm minimum of empty carrier tape sealed with cover tape. The entire carrier tape must release from the reel hub as the last portion of the tape unwinds from the reel without damage to the carrier tape and the remaining components in the cavities.

More details can be found in the Alcatel Microelectronics document spec 16665 and spec 9210.

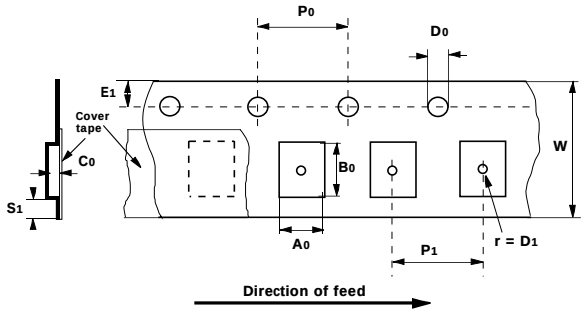


Fig. 15

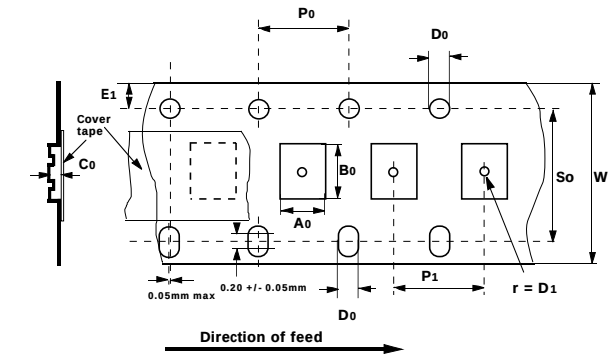


Fig. 16

Tooling list for carrier tape:

Package Type	Tape width (W)	Pitch mm (P1)	A0 mm	B0 mm	C0 mm	Standard Qty/reel	Meters /reel	Cavity /reel
SO16 B	16 mm	12	10.7	10.7	3.1	1000	13.0	1083

6. Soldering information

All components meet the minimum requirments of the two requirements outlined below.

- Solder wettability : test Mil STD 883 D method 2003 (95 % solder wetting of the leads)

- Wetting balance solderability test : Mil SRTD 883 D method 2022 (5 sec 245 °C)

Through hole devices

These devices can be soldered with most industry standard soldering processes.
The devices withstand the resitance to soldering test IEC 68 - 2 - 20 (2 cycles).

Surface mount devices

Take into account the dry pack recommendatinos as stated on the label applied.

All SMD components can be soldered with the standard infra red, vapour phase and double wave soldering processes. Recommended profiles can be found in fig 17, 18 and19.

IR surface mountable components meet the following test sequence

storage 85 °C, 85 % RH, 168 hrs followed by 2 cycles of infra red solder heat application (CECC00802) and 100 thermal cycles -55 °C / + 125 °C (Mil STD 883 D method 1010).

Double wave mountable components meet the following test sequence

storage 85 °C, 85 % RH, 168 hrs followed by 1 cycles of double wave solder heat application (CECC00802) and 100 thermal cycles -55 °C / + 125 °C (Mil STD 883 D method 1010).

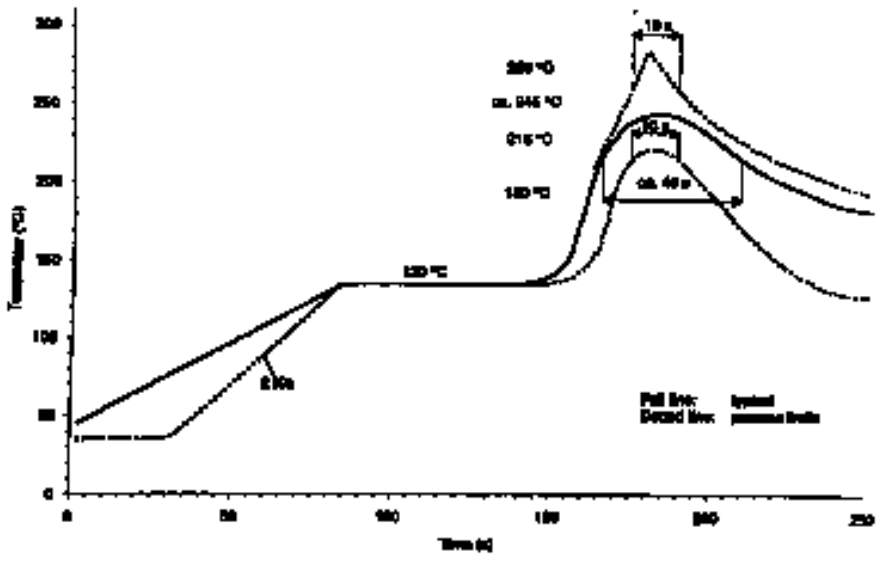
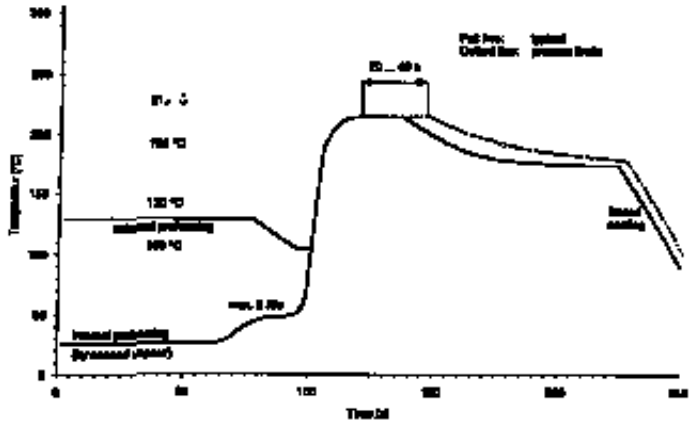


Fig. 17: Infra Red Soldering



Vapour phase; batch system with pre heating

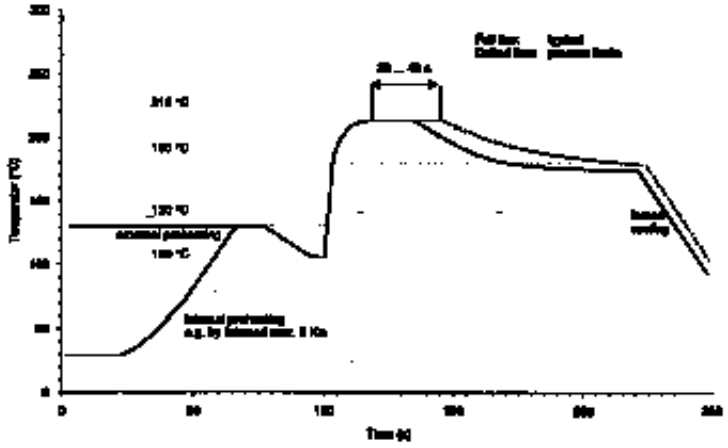


Fig. 18: Vapour phase; in line system with pre heating

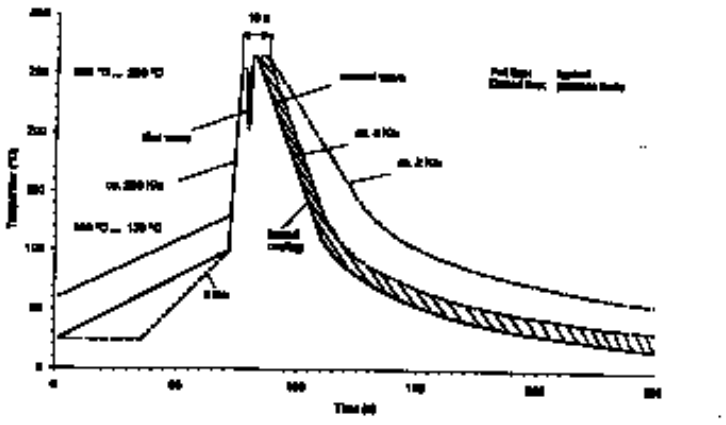


Fig. 19: Double Wave Soldering

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
TB	Storage temperature	- 55	150	°C
Vbat	Power supply voltage	- 0.3	50	V
Vi1	Voltage at input SleepB	- 0.3	Vbat	V
Vi2	Voltage at input WU	- 2.0	24	V
Vi3	Voltage at input DE	- 0.3	V56	V

Operating Ranges

Symbol	Description	Min	Max	Unit
TA	Ambient temperature	- 40	125	°C
Vbat	Power supply voltage	6.1	16.0	V
Ivbat	Current consumption (note1)		14	mA
Vbatr	Power supply voltage for operation with reduced performance (note 2)	16	24	V

Note 1:
The current consumption will be measured under the following conditions :
- pin V56 not loaded resistively
- pin Vpol not loaded resistively
- DE = '1' (i.e. is left open).
- pins Data and DataB not loaded resistively
- pins R0,R1 and R2 not loaded resistively

Note 2:
Within this range the following parameters will degrade : Ivbat, Ifv, Iuc, Ilm, Ils. These parameters will not be tested within this operating region.

Detailed Electrical Characteristics

All characteristics are valid under the full operating range of temperature and supply voltage, mentioned above, unless otherwise noted.
The pin CS has to be connected to ground via an external resistor of 10 KΩ (tol. < 1%).
Characteristics marked with § are not tested in production.

Sleep / Wake-up System

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vrev1	Voltage drop from Vbat to DataB (master node)	0		1	V	Vbat between 10 and 16 V Irev1 = 5mA
Vrev2	Voltage drop from DataB to WU (slave node)	0		2	V	VDataB between (10·Vrev1) and (16·Vrev1) V Irev2 = 5 mA
Vrev	= Vrev1 + Vrev2	0		3	V	
Idetect	Wake up detection current	10		15	mA	
ZKio §	Impedance of an open switch	1			MΩ	
TKi §	Delay time for switches			10	µs	
ICR	Short circuit current	15			mA	
tds	Delay time for Idetect	1		10	ms	C at pin WU = 10 nF
Ifv	Current consumption of a slave node in sleep mode (current from DataB to Gnd)			30	µA	VDataB between 10 and 12 V
Iuc	Current consumption of a master node in sleep mode (current from Vbat to Gnd)			150	µA	Vbat between 10 and 12 V

Voltage Regulator

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V56	Regulated output voltage	5.22	5.6	5.88	V	Resistive load between 0 and Ial Cap. load ≥ 10 µF
Ial	Maximum external load			30	mA	
tal	Settling time after enabling regulator			10	ms.	Cap. load = 10µF Res. load < 30 mA
Isc	Short circuit current	30			mA	
Z56 §	Output impedance in sleep mode	7	14	21	KΩ	note 1
V56S	Output voltage in sleep mode			0.5	V	

Note 1:
When in sleep mode, the pin V56 is internally connected to a pull down resistor of ± 14 KΩ in parallel with the active circuit which is normally supplied with the voltage V56. Therefore the exact output impedance is undefined and therefore not measured.

Transmitter

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vod	differential output voltage	6.4			V	square wave at DE : - Freq = 20 KHz - duty cycle = 50 % note 1
Vmce	common mode voltage (DC condition)			6.6	V	Vbat = 12 V
Dvmcei	variation of the common mode voltage within 2us after DE transition	-3		3	V	fig.18 square wave at DE : - Freq = 20 KHz. - duty cycle = 50 %
Dvmcef	variation of the common mode voltage 2us after DE transition	-1		1	V	fig.18 square wave at DE : - Freq = 20 KHz. - duty cycle = 50 %
IldD	current limitation in dominant mode at pin Data	40	50	64	mA	VData = V56
IldDB	current limitation in dominant mode at pin DataB (absolute val.)	40	50	64	mA	VDataB = GND
Ilr	current limitation in recessive mode (absolute value for Data)	1	1.2	1.45	mA	note 2
Mim	matching of dominant currents	0		+30	%	note 3
Mir	matching of recessive currents	0		+30	%	note 4
IRG1	Recessive current template level 1	Ilr -20%		Ilr +20%	mA	fig. 16a fig. 16b
IRG2	Recessive current template level 2	-0.5		0.2	mA	fig. 16a fig. 16b
IDG1_D	Dominant current template level 1 for Data	ILdD -35%		ILdD +20%	mA	fig. 16b
IDG1_DB	Dominant current template level 1 for DataB	ILdDB -40%		ILdDB +20%	mA	fig. 16a
IDG2	Dominant current template level 2	-8		2	mA	fig. 16a fig. 16b
Ilm	leakage current for master node at (Data + DataB)			60	µA	note 5
Ils	leakage current for slave node at (Data + DataB)			40	µA	note 5
IFD12	leakage current at pin Data	-50		50	µA	0V< VData<15V 0<Vbat<0.5V

continued

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
IFD3	leakage current at pin Data	-750		1600	µA	-15V< VData<0 Vbat=V56=0
IFDB12	leakage current at pin DataB	-50		50	µA	0V< VDataB<15V 0<Vbat<0.5V
IFDB3	leakage current at pin DataB	-750		1600	µA	-15V< VDataB<0 Vbat=V56=0
Dtpdr1	Absolute value of difference between propagation delay times tpdrlh1(data) and tpdrhl9(datab) for D>R transition	-250		250	ns	fig 15
Dtpdr9	Absolute value of difference between propagation delay times tpdrlh9(data) and tpdrhl1(datab) for D>R transition	-1000		1000	ns	fig 15
Dtprd1	Absolute value of difference between propagation delay times tprdlh1(datab) and tprdhl9(data) for R>D transition	-250		250	ns	fig 15
Dtprd9	Absolute value of difference between propagation delay times tprdlh9(datab) and tprdhl1(data) for R>D transition	-1000		1000	ns	fig 15
tpdrlh1 tpdrhl9	Propagation delay D->R	50		500	ns	note 6, fig. 15
tpdrlh5 tpdrhl5	Propagation delay D->R	300		1150	ns	note 6, fig. 15
tpdrlh9 tpdrhl1	Propagation delay D->R	550		1800	ns	note 6, fig. 15
tprdlh1 tprdhl9	Propagation delay R->D	100		600	ns	note 6, fig. 15
tprdlh5 tprdhl5	Propagation delay R->D	200		1150	ns	note 6, fig. 15
tprdlh9 tprdhl1	Propagation delay R->D	350		1800	ns	note 6, fig. 15

Note 1:
Vod = Abs (VData - VDataB)DE=0 + Abs (VData - VDataB)DE=1
This is a peak to peak measurement.

Note 2:
The current limitation in recessive mode is measured with Data connected to GND, and DataB to V56.

Note 3:
Mim = |(2 * (IData - IDataB))| / (|IData |+ |IDataB|)

Note 4:
Mir = |(2 * (IDataB - IData))| / (|IData| +| IDataB|)

Note 5:
The pins Data and DataB are resistively connected to each other via the integrated receiver filter. Defining a leakage current at these nodes therefore only makes sense when the voltages at these two nodes are forced at the same voltage, so that no current is flowing through the filter.
As a consequence of this the definition of leakage currents on pins Data and DataB only makes sense when the line transmitter is disabled, i.e. in sleep mode.
When the device is in sleep mode, the pin DataB is connected via a switch either to Vbat or to the pin WU.
Therefore the leakage currents are defined as follows :
- the pins Data and DataB are connected to each other and the sum of the leakage current is measured.
- for Ilm :
  Vbat = 12 V
  V (Data + DataB) = 12 V
- for Ils :
  Vbat = 0 V
  V (Data + DataB) = Vwu = 12 V

Note 6:
During these measurements the load at Data and DataB is :
R->D : 4.3 nF to GND + 20 mA to simulate the total recessive load at a node
D->R : 270 pF to GND

Note 7:
Dtprd production test limit =100ns
design limit = 50ns

Note 8:
These limits are design limits, but will not be tested in production

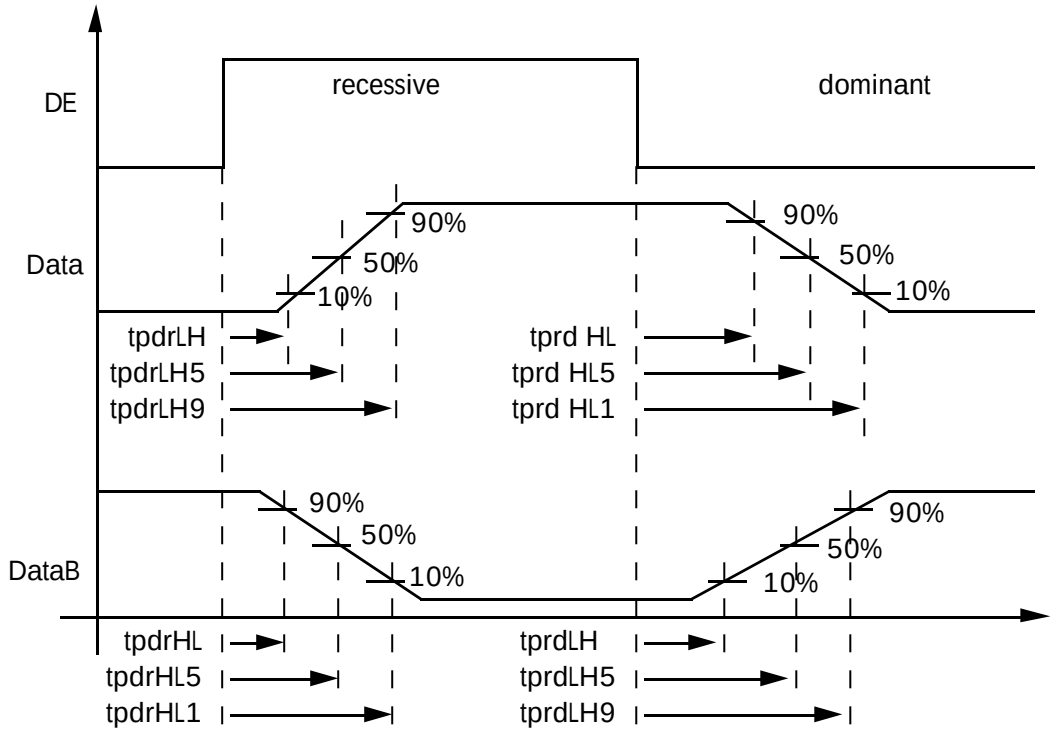


Fig.20: Level Dependent Delays

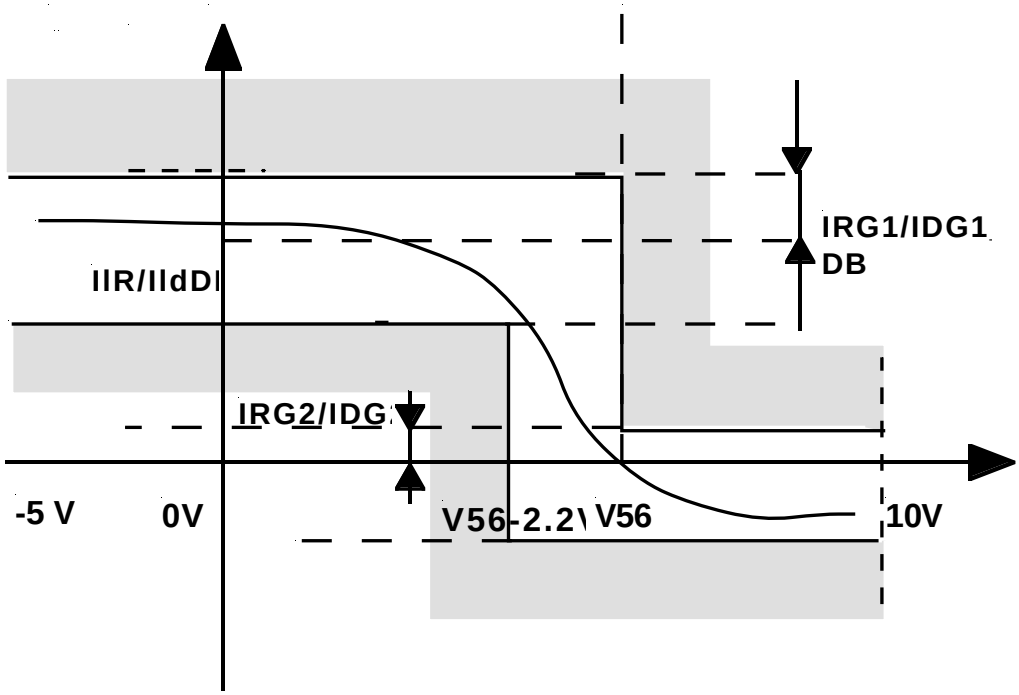


Fig. 21a: Current Gabaryt

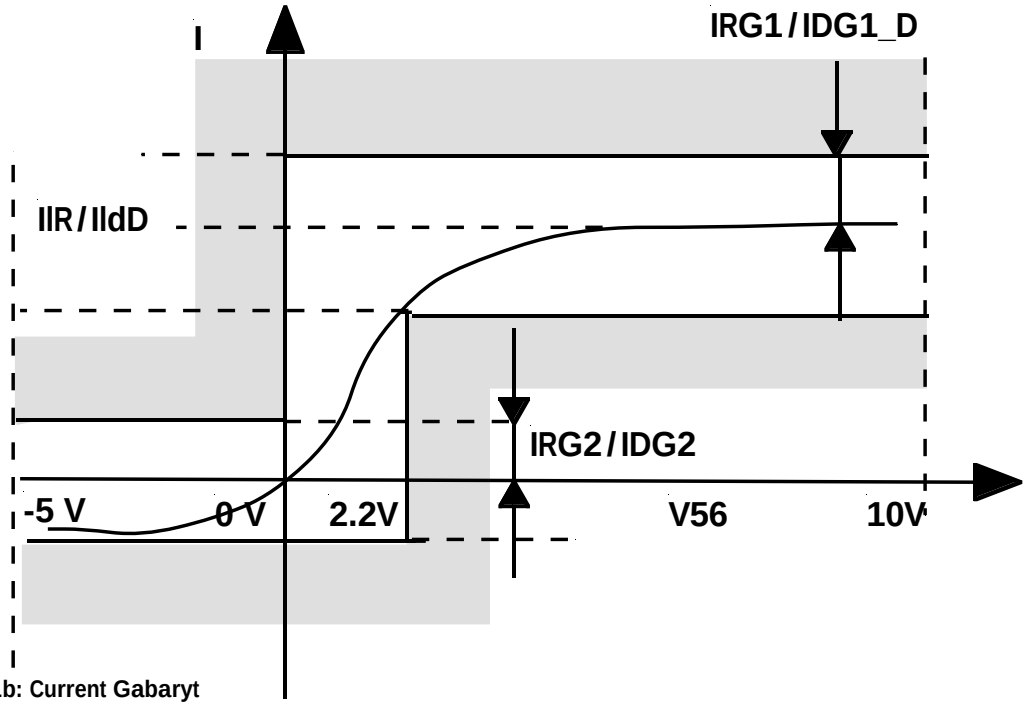


Fig.21b: Current Gabaryt

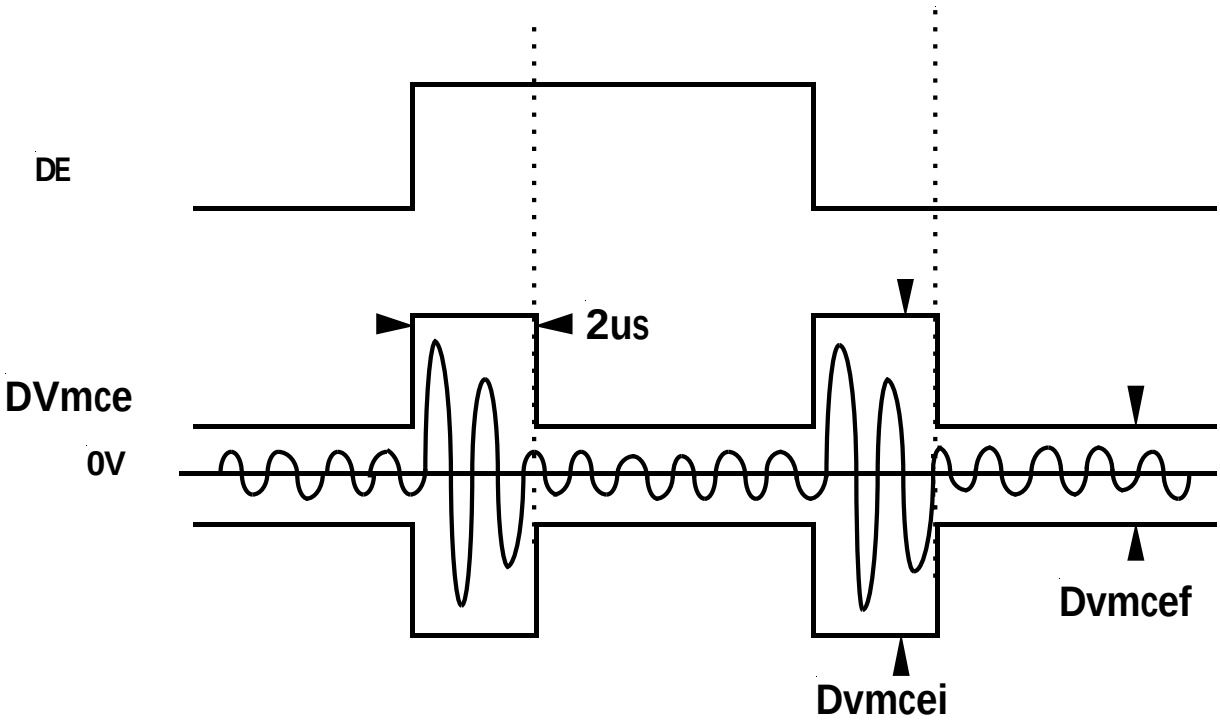


Fig.22: Transmitter Propagation Delays

Receiver

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vmcr	Common mode voltage range	-2.8		6	V	
Fr1 §	Resistor value R1 in filter	21	42	72	KΩ	Fig. 4 note 1
Fr2 §	Resistor value R2 in filter	14	28	48	KΩ	Fig. 4 note 1
Fr12 §	Ratio Fr2/Fr1 = 42/28					Fig. 4 note 1
Dfr21 §	Tolerance on FR12	-1		+1	%	Fig. 4 note 1
Fc1 §	Capacitor value C1 in filter	8.5	10	11.5	pF	Fig. 4 note 1
VCP	Positive comparator threshold level	200		420	mV	note 2
VCN	Negative comparator threshold level	- 420		- 200	mV	note 2
Voff	Input offset voltage	-50		+50	mV	note 2
Vhyst	input hysteresis	480		750	mV	note 2
TprLH, TprHL	Propagation delay time from input input (Data, DataB, Vpol) to output (R0 or R1 or R2)			600	ns	Vin peak-peak = 1 V note 3
Dtpr	Difference between propagation delay times			100	ns	Vin peak-peak = 1 V
Zgt1 §	Output impedance of pin Vpol			200	Ω	at 1 MHz
Zgt2	Output impedance of pin Vpol			200	Ω	at 250 KHz
Vgt	Output voltage of pin Vpol	2.51	2.65	2.79	V	load current < 4mA

Note 1:
Matching of resistors and capacitors of the filters on the two inputs is better than 1%.
The different elements of the input filter cannot be measured externally. During production test the following parameters will be measured: the total resistance (Fr1+Fr2) between pin Vpol and Datax. These measurements, combined with the measurements on hysteresis, offset and propagation delays will guarantee the correct operation of the receiver section.

Note 2:
The values for positive and negative threshold level, offset and hysteresis of the line receiver are specified at the pins Data and DataB. This is a combination of the actual hysteresis and offset of the comparator, and the ratio of the resistors in the input filter.
Vhyst is defined as (VCP- VCN)
Voff is defined as (VCP+VCN)/2.

Note 3:
To measure the comparator with output R0, Data will be driven with a voltage Vpp1 = 1 V, DataB will be driven with Vpp2 = 1 V Vpp1 and Vpp2 are complementary.
To measure the two other comparators, Datax will be driven with a voltage Vpp = 2 V, and centered around the level Vpol.

Digital Inputs/Outputs

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vil	Input level low for input DE	1			V	
Vih	Input level high for input DE			4	V	
VsleepB	Threshold level for input SleepB	3.5	4	4.5	V	
RsleepB	Pull down resistor at input SleepB	5	10	18	KΩ	
Rde	Pull up resistor at input DE	1.8	3.3	5.5	KΩ	
Vol	Output level low for outputs R0, R1, R2			1	V	Iout = 2 mA
Voh	Output level high for) outputs R0, R1, R2	4		V56	V	Iout = 2 mA
TdLH, TdHL	Rise and fall time at outputs R0, R1, R2			50	ns	load: · R = 1 MegΩ · C = 20 pF
Dtd	Difference between rise and fall time			25	ns	

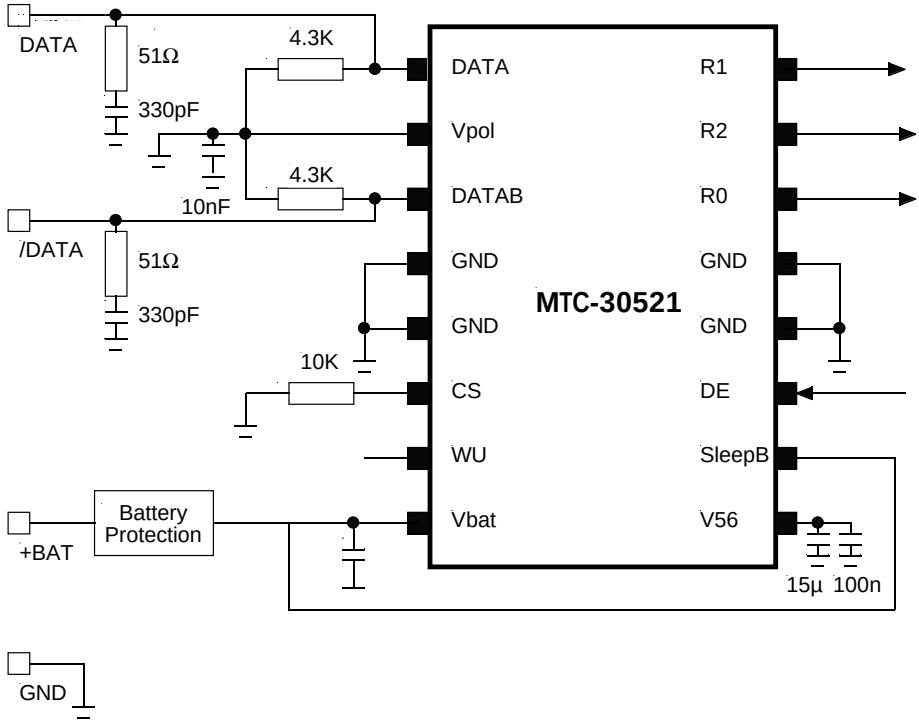


Fig. 23: REMQ Applications diagram

Quality and Reliability

Reliability Performance

The Intrinsic Failure Rate

When used under benign conditions and a junction temperature of 50°C, the failure rate will not exceed :

- 400ppm during the first year in the field
- 100 FIT or ppb/hour after the first year (long term failure rate)

Failures due to external overstress such as ESD, voltage and current overstress (e.g. due to EMI), mechanical and thermal shocks, ... are not included in these figures.

External Stress Immunity

- Electrostatic discharges :

  The device withstands 1000 Volts Standardized Human Body Model ESD pulses when tested according to MIL std 883c method 3015.5 (pin combination 2)

- Latch-up :
  Static latch-up protection level is 100mA at 25°C when tested according to JEDEC standard EIA/JESD78.

The Useful Life

The useful life, when used under moderate conditions, is at least 10 years. The term useful life is specified as the point in the lifetime, where the intrinsic failure rate exceeds the long term failure rate specified under the paragraph: 'The Intrinsic Failure Rate'.

Quality

Lot-by-lot Acceptance Tests

Test	Conditions	Inspection lev	AQL level
Functional and parametric	To detail specification Tamb =25°C (Full temperature range performance guardband)	II	0.04%
External visual	Correctness of marking No physical damage to body or leads Major Minor (cosmetic)	 II II	 0.15% 2.50%
Hermeticity	(Not applicable to non cavity packages) Fine leak Gross leak	 II II	 0.40% 1.00%
Solderability	T=245°C Min. 95 % wetting of terminations	S-4	1.00%
Dimensions	Major dimensions to detail specification	S-4	1.00%

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury.

Alcatel Microelectronics customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Alcatel Microelectronics for any damages resulting from such improper use or sale.

MTC-30521

Alcatel Microelectronics
info@mie.alcatel.be
http://www.alcatel.com

Sales Offices

Central Europe
Arabellastraße 4
81925 München
Deutschland
Tel. +49 89 920 07 70
Fax +49 89 910 15 59

Stuttgart Office
Walter-Koch-Straße 38
74189 Weinsberg
Deutschland
Tel. +49 7134 900 810
Fax +49 7134 900 811

Northern Europe
Raketstraat 62
1130 Brussels
Belgium
Tel. +32 2 728 18 11
Fax +32 2 726 42 15

Sales & Design Centres

Italy
Via Trento 30
20059 Vimercate MI
Italy
Tel. +39 39 686 4520
Fax +39 39 686 6899

Southern Europe
10, rue Latécoère, B.P.57
78140 Vélizy Cedex
France
Tel. +33 1 46 32 53 86
Fax +33 1 46 32 55 68

USA
M/S 412-115
1225 N. Alma Road
Richardson
TX 75081-2206
Tel. (972) 996 2489
Fax (972) 996 2503

Representatives

Northern Germany
TRIAS
Moerser Landstraße 408
47802 Krefeld
Tel. +49 2151 95 30 111
Fax +49 2151 95 30 115

Taiwan ROC
Alcatel ITS Ltd
Suite D, 8th floor 133
Section 3, Min Seng E. Road
Taipei 015, Taiwan
Tel. +886 2 717 1255
Fax +886 2 717 1250

Japan
Alcatel ITS Japan Ltd
Yubisu Garden Plae Tower 24
20-3 Ebisu 4-chrome, Shibuyaku
Tokyo, 150, Japan
Tel. +81 3 5424 8561
Fax +81 3 5424 8581

Marketing & Design Centre

Raketstraat 62
1130 Brussels
Belgium
Tel. +32 2 728 18 11
Fax +32 2 726 42 15

Headquarters Manufacturing & Customer Service

Westerring 15
9700 Oudenaarde
Belgium
Tel. +32 55 33 24 70
Fax +32 55 33 27 68

USA

Premier Technical Sales
SAN DIEGO, CA, 2011 Via Tiempo, Cardiff, CA 92007, Tel. (760) 943 6222, Fax (760) 943 0425
SANTA CLARA, CA, 3235 Kifer Road, Suite 110, Santa Clara, CA 95051, Tel. (408) 736 2260, Fax (408) 736 2826
TUSTIN, CA, 2660 Walnut Ave, Unit H, Tustin, CA 92680, Tel. (714) 573 8242, Fax (714) 573 4942
ATLANTA, GA, 135 Arden Way, Peachtree City, GA 30269, Tel. (770) 632 9648, Fax (770) 486 4098
BOSTON, MA, 33 Boston Post Road West, Suite 270, Marlboro, MA 01752, Tel. (508) 460 1730, Fax (508) 460 1731
PORTLAND, OR, 5319 S.W. Westgate Dr. Suite 136, Portland, OR 97221, Tel. (503) 297 3956, Fax (503) 297 4956
AUSTIN, TX, 12148 Jollyville Road, Unit 422, Austin, TX 78759, Tel. (512) 257 8218, Fax (512) 257 1714
DALLAS, TX, 800 East Campbell Road, Suite 199, Richardson, TX 75081, Tel. (972) 680 5233, Fax (972) 680 5234
OTTAWA, ONTARIO, CANADA, 43 Pretty Street, Stittsville, Ontario, K2S1A4 Canada, Tel. (613) 836 1779, Fax (613) 836 4459

12/97-DS0258 a